5E 5102

5E 5102

B.Tech. V Semester (Main & Back) Examination, Nov./Dec. - 2017
Computer Science and Engineering
5CS2A Digital Logic Design

Time : 3 Hours

Maximum Marks : 80
Min. Passing Marks : 26

Instructions to Candidates :

Attempt any five questions, selecting one question from each unit. All Questions carry equal marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly). Units of quantities used/calculated must be stated clearly.

Unit - I

1. a) Explain lexical elements of VHDL language with example. (8)

   b) Explain mixed style of modeling with example. (8)

OR

1. a) Describe the design steps of digital circuit using HDL. (8)

   b) Write down a behavioural style code for half subtractor. (8)

Unit - II

2. a) Explain different kinds of subprogram with examples. (8)

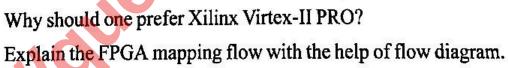   b) Write the differences between package and entity. (8)

OR

2. Explain the following statements with one example in VHDL : (16)

   a) If statement

   b) Case statement

   c) Loops statement

   d) Generate statement

Unit - III

3. a) Write a VHDL code for serial adder circuit. (8)

   b) Write VHDL code for rising edge J-K flip-flop by using structural modeling. (8)

(1)

[Contd....

3. a) Explain the following :   (4×2=8)

      i)   Clock skew

      ii)   Metastable state

      iii) Hold Time

      iv) Set up time

  b) Write a short note on :   (4×2=8)

      i)   ROM

      ii)   FPGA

Unit - IV

4. a) Define event driven circuits and write steps for designing these circuits. (10)

  b) What is meant by race-free assignments?   (6)

OR

4. a) Explain in detail essential hazards and eliminating hazards.   (8)

  b) Explain the procedure of state reduction of incompletely specified machine with a suitable example.   (8)

Unit - V

5. a) Write short notes on :   (4×2=8)

      i)   SRAM

      ii)   Flash Memory

  b) What is the importance of Altera static   (8)

OR

5. a) Why should one prefer Xilinx Virtex-II PRO?   (8)

  b) Explain the FPGA mapping flow with the help of flow diagram. (8)