4E2110

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# 4E2110

**B. Tech. (Sem. IV) (Main / Back) Examination, June/July - 2013**
**Electrical Engg.**
**4EE2 Digital Electronics**

Time : **3** Hours] [Total Marks : **80**
[Min. Passing Marks : **24**

*Attempt any **five questions**. Selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

Use of following supporting material is permitted during examination.
*(Mentioned in form No. 205)*

1. NIL 2. NIL

## UNIT - I

1 (a) Convert the following :

(i) $(36.625)_{10}=(?)_2$

(ii) $(1011011.10)_2=(?)_8$

(iii) $(2DE \cdot CA6)_{16}=(?)_{10}$

(iv) Convert the given BCD code (natural) in Excess-3 code.
100101110101

8

(b) Explain the following with suitable example.

(i) Sign Magnitude Representation

(ii) BCD arithmatic

8

OR

1 (a) Find the redix value if :
$(23)_r+(12)_r=(101)_r$

3

(b) Find using r's complement method.

$(BLA5)_{16}-(29DA)_{16}$

3

(c) Make notes on the following :

(i) Natural BCD and ASCII codes.

(ii) Error detecting and correcting codes.

10

## UNIT - II

2 (a) Draw all logic gates with their truth tables. Generate X-OR gate with any one universal gate.

6

(b) Reduce the expression using mapping and implement if in universal logic.

$\Pi M(2,8,9,10,11,12,14)$

6

(c) Simplify the expression using boolean algebra.

$$\overline{\overline{A\bar{B}+ABC+A(B+A\bar{B})}}$$

4

**OR**

2 (a) Simplify using K-map.

$f=\Sigma m(1,3,7,11,15)+d(0,2,5)$

5

(b) Explain De Morgan's law and Duality theorem.

5

(c) Explain following with example.

(i) SOP and POS form

(ii) Minterm and Maxterm

6

## UNIT - III

3 (a) Draw and explain the circuit diagram of a TTL-NAND gate with totempole output. 8

(b) Define the following terms :
(i) Propagation Delay
(ii) Power Dissipation
(iii) Fanout
(iv) Noise Margin 8

**OR**

3 (a) Explain the working of CMOS-NAND and NOR gates. 8

(b) Explain the following briefly : 
(i) RTL
(ii) ECL
(iii) FET as a switch
(iv) 3-state output logic 8

## UNIT - IV

4 (a) Explain full subtractor in detail. Realize it with two half-subtractors. 8

(b) Explain 1:4 demultiplexer. Design 1:8 DEMOX using two 1:4 DEMOX. 8

**OR**

4 (a) Design a 4-bit parallel adder using full adders. 6

(b) Implement the following boolean function using 8:1 MUX.

$F(A,B,C) = \Sigma m(1,3,5,6)$ 6

(c) Describe encoders and decoders with suitable diagram. 4

## UNIT - V

5 (a) Discuss Master-Slave PK-Flip Flop. Also realize PKFF using D-Flip Flop. 8

(b) Make a detailed note on counters. 8

OR

5 Make short notes on any four of the following :

(i) D-Flip Flop

(ii) P-Flip Flop

(iii) Shift Register

(iv) R-S latch

(v) Race around condition 16