4E2110

Roll No. _____ Total No of Pages: 4

4E2110

B. Tech. IV Sem. (Back) Exam., June/July-2014

Electrical Engineering

4EE2 Digital Electronics

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks: 24

Instructions to Candidates:-

*Attempt any **five questions**, selecting **one question** from **each unit**. All Questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/ calculated must be stated clearly.

Use of following supporting material is permitted during examination.

(Mentioned in form No. 30)

1. _____ 2. _____

UNIT I

Q.1 (a) Explain the following codes with example - [10]

(i) 8421 code

(ii) 2421 code

(iii) Reflective code

(iv) Sequential code

(b) Convert $[10110]_2$ to Gray code. [6]

OR

Q.1 (a) Construct Hamming code for BCD 0110. Use even parity [8]

(b) For ASCII Code -

(i) Determine the number of panty bits which must be appended to the code to make it an error –correcting code i, e Hamming code.

(ii) Determine the locations of the parity bits. [8]

UNIT-II

Q.2 (a) You have rented a locker in a bank. Express the process of opening the locker in terms of a digital operation. [8]

(b) Which of the following system are analog & which are digital? Why? [8]

(i) Pressure gauge

(ii) An electronic counter used to count persons entering an exhibition

(iii) Clinical thermometer

(iv) Electronic calculator

(v) Transistor radio receiver

(vi) Ordinary electric switch

(vii) Electronic Voting Machine (EVM)

(viii) Multimeter

OR

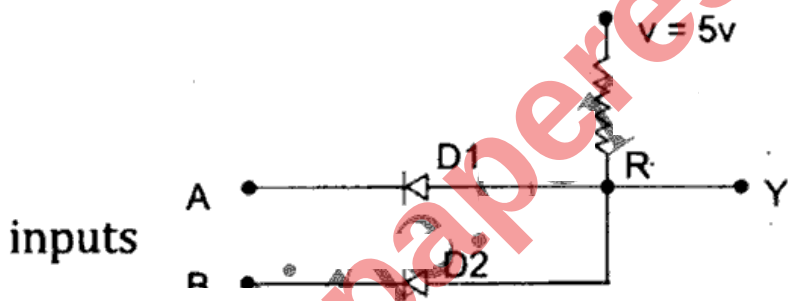
Q.2 (a) Simplify the logic function of following equation using the Quine Mc Cluskey method -

$f(A,B,C,D) = \sum m\ (1,3,7,11,15) + d\ (0,2,5)$ [10]

(b) How will you group eight adjacent ones? [6]

UNIT- III

Q.3 (a) In the diode circuit of figure, the inputs applied are 0 V & 5 V corresponding to low & high respectively.



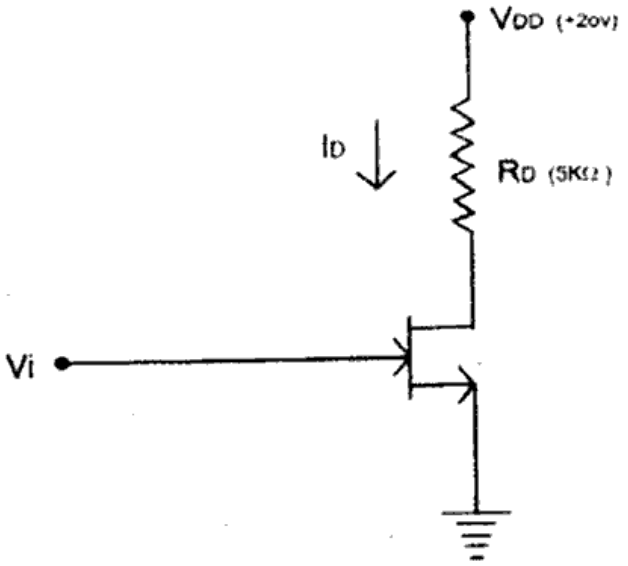
(i) Determine output Y for all the possible combination of inputs [6]

(ii) Does it perform any logic function? If yes, name the logic function. [6]

(b) Draw the diagram of 3 input TTL NAND Gate driving N similar Gates [4]

OR

Q.3 (a) For the circuit shown in figure determine the output voltage V_o for the input voltage V_i of (a) -5V (b) 0V. The output characteristics of the JFET are modified. Draw the changed characteristic. [8]



(b) Write short note on CMOS Logic families [8]

UNIT- IV

Q.4 (a) Design a 32:1 multiplexer using 16:1 multiplexers & one OR gate. [6]

(b) Write dawn the algorithm for performing subtraction using adder. [10]

OR

Q.4 (a) Design a hexadecimal- to – binary encoder using 74148 encoders & 74157 multipliers. [10]

(b) Write a shat note on parity generators. [6]

UNIT V

Q.5 (a) Design a sequence generator to generate the sequence ------ 1101011------. [10]

(b) Design a divide – by -6 counter using 7490. [6]

OR

Q.5 (a) Design a 3 – bit synchronous counter using J-K Flip – Flops. [10]

(b) Design a counter with states 0011 through 1100 using 74169 counter. [6]
