5E3124

Roll No. : _____ Total Printed Pages : 3

5E3124

B. Tech. (Sem. V) (Main/Back) Examination, December - 2013
Electrical Engg.
5EE2 Microprocessors and Computer Architecture

Time : 3 Hours] [Total Marks : 80
[Min. Passing Marks : 24

Attempt any five questions, selecting one question from each Unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used / calculated must be stated clearly.

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. NIL 2. NIL

UNIT - I

1 (a) Briefly explain the bus structures in 8085 microprocessor based circuits.
(b) Explain the programmed I/O data transfer.
(c) Differentiate between static and Dynamic memories.
(d) Explain the concept of physical and virtual memory. 4×4=16

OR

1 (a) Draw the memory map and block schematic of an 8085 based system having following specifications.
(i) 32 KB of program memory
(ii) 16 KB of data memory. 8

(b) Differentiate between absolute address decoding and linear select address decoding. 8

UNIT - II

2 (a) How does the Demultiplexing of Address Bus and Data bus takes place in 8085 microprocessor ? Explain. 8

(b) Draw and explain the timing diagram of fetch cycle of 8085 microprocessor with suitable example. 8

OR

2 (a) Differentiate between :
(i) Vectored and non-vectored interrupts
(ii) Edge-triggered and level-triggered interrupts.

8

(b) What are the various software interrupts in 8085 microprocessor ? Give their vector location in IVT.

8

UNIT - III

3 (a) Write 8085 assembly language program to store the contents of the Flag register in memory location 2000 H and load the flag register from Top of stack.

8

(b) Illustrate RIM and SIM instructions. Explain how these instructions can be used for serial data handling.

8

OR

3 (a) Describe the sequence of events that are followed for execution of PUSH and POP instructions in 8085 M.P.

4

(b) Explain the following instructions in Instruction set of 8085 MP.
(i) DAA (ii) DAD
(iii) PCHL (iv) RAL.

4

(c) Explain the syntax of different jump instructions in 8085 MP.

4

(d) Enumerate the data transfer instruction group of 8085 MP.

4

UNIT - IV

4 (a) Describe the response that an 8259 will make if it receives an interrupt signal on its IR3 and IR5 inputs at the same time. Assume fixed priority for the IR inputs. What response with the 8259 make if it is servicing an IRS interrupt and an IR3 interrupt signal occurs.

8

(b) Enumerate the sequence of instructions that you need to send to 8279 interfaced to 8085 MP to display 8888.

8

OR

4 (a) Interface a 4×4 keyboard using two 8255 ports and write a 8085 assembly language program to read the code of a pressed key. 8

(b) Explain why 8255 ports are divided into two groups ? Discuss how these groups are controlled in different modes of operation. 8

UNIT - V

5 (a) With the help of basic cell explain SRAM and DRAM. Discuss the advantages and disadvantages of the above memories. 8

(b) Explain the following terms with reference to DRAM
(i) Write cycle
(ii) Access time
(iii) Refresh
(iv) Read cycle. 8

OR

5 (a) Explain the following data transfer schemes.
(i) Interrupted I/O
(ii) DMA 8

(b) Explain the following terms :
(i) Memory seek time
(ii) Memory band width
(iii) Memory latency
(iv) Memory Hierarchy. 8
