Roll No. | | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech.(Electronics Engg.) (2012 Onwards)
B.Tech.(ECE/Electronics & Computer Engg./ETE) (2011 Onwards)
(Sem.–3)

DIGITAL CIRCUIT AND LOGIC DESIGN

Subject Code : BTEC-302
Paper ID : [A1131]

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Write briefly :

a) Subtract the following numbers :

i) $(BC5)_{16} - (A2B)_{16}$ ii) $(175.6)_8 - (47.7)_8$

b) Why 2's complement is used in computers for representation of negative numbers?

c) Prove that $(A + \bar{B} + AB)(A + \bar{B})(\bar{A}B) = 0$

d) Prove that a dual of XOR is also its complement.

e) How can a DEMUX be used as a decoder?

f) What is race around condition?

g) What is flip flop?

h) What are the applications of universal shift registers?

i) What is the MOD number of 6-bit counter?

j) Which is the fastest logic family and why?

SECTION-B

2. Minimize the following expression using K-map :

   $f(A,B,C,D,E,F) = \sum m(0,5,7,8,9,13,23,24,25,28,29,37,40,41,42,43,55,56,57,60,61)$

3. Implement the following function using 16:1 multiplexer

   $f(A,B,C,D,E) = \sum m(2,4,5,7,10,14,15,16,17,25,26,30,31)$

4. Design a Gray to Excess-3 code converter using NOR gates only.

5. Determine the reduced state table equivalent of the following table

Present State	X = 0		X = 1	
	Next State	Output	Next State	Output
1	1	0	1	0
2	1	1	6	1
3	4	0	5	0
4	1	1	7	0
5	2	0	3	0
6	4	0	5	0
7	2	0	3	0

6. Design a Modulo-5 ripple counter using 3-bit ripple counter.

SECTION-C

7. What is the need of ADC? Explain in detail the single slope integrating type ADC.

8. a) How many 256×8 memory chips are required to obtain a 2048×8 memory? Show the memory addresses associated with each memory chip.

   b) What limits the speed of TTL gate? How can the speed of TTL gate be enhanced?

9. a) A combinational logic is defined by :

   $F_1(A,B,C) = \sum m(3,5,6,7)$

   $F_2(A,B,C) = \sum m(0,2,4,7)$

   Implement the circuit with PLA having 3-inputs, 4 product terms and two outputs.

   b) What is the need of encoder? Explain in detail the operation of priority encoder.