

5E5102

Roll No. 13E2205732

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5E5102

B. Tech V Sem. (Main/Back) Exam. Nov-Dec. 2015
Computer Science & Engineering
SCS2A Digital Logic Design

Time: 3 Hours

Maximum Marks: 80

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

Instructions to Candidates:

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination.

1. NIL

2. NIL

UNIT-I

- Q.1 (a) What are various levels of abstraction in VHDL? Also explain its structure. [8]
(b) What are the Basic Modeling Constructs in VHDL? [8]

OR

- Q.1 (a) What are the Data Types in VHDL? Explain with example. [8]
(b) Write VHDL code for ripple carry adder and draw its simulation waveform. [8]

UNIT-II

- Q.2 (a) Describe the sub programs and explain types of sub programs. [8]
(b) Describe the resolved signals with suitable example. [8]

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OR

- Q.2 (a) Explain packages and use clauses of VHDL language. [8]
(b) Compare the component declaration and component instantiations. [8]

UNIT-III

- Q.3 (a) What are clocked sequential circuits? Give some examples of clocked sequential circuits. [8]
(b) What is the difference between Moore and mealy state machines? [8]

OR

- Q.3 (a) Describe conversion of ASM charts to hardware with a suitable example. [8]
(b) Explain concept and working of FPGA and PLD. [8]

UNIT-IV

- Q.4 (a) Explain the stable and unstable states and explain the reduction of the basic state table. [8]
(b) Explain the race free assignment by using K-map of four state variables. [8]

OR

- Q.4 (a) Define Event Driven Circuits and write steps for designing these circuits. [8]
(b) What is the difference between Dynamic hazards and Functional hazards? [8]

UNIT-V

- Q.5 (a) Describe the logic block and interconnection in the FPGA architecture and explain the nearest neighbor connectivity. [8]
(b) What are different approaches to achieving programmability? [8]

OR

Q.5 Write short notes on following:-

- (a) SRAM [8]
(b) Flash Memory [8]