5E5102

Roll No. _____ Total No of Pages: 2

5E5102

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016

Computer Engineering

5CS2A Digital Logic Design

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 Explain Hardware Description Languages and their use in digital logic design in detail along with their application areas. [16]

OR

Q.1 (a) Describe scalar date types & operations in VHDL. [8]

(b) Explain scalar date types & operations in VHDL. [8]

UNIT – II

Q.2 Write Technical notes on following -

(a) Packages & Use Clauses in VHDL. [8]

(b) Components & configurations in VHDL. [8]

OR

Q.2 What are concurrent statements in VHDL. Also explain use of VHDL in simulation and synthesis of digital circuits with example. [16]

UNIT – III

Q.3 (a) Write and explain design steps for synchronous sequential circuits. [8]

(b) Write short note on programmable logic devices in detail. [8]

OR

Q.3 Explain the process of converting ASM charts to hardware and also explain Algorithmic state charts in detail along with concept of set-up time and hold time. [16]

UNIT – IV

Q.4 Explain in detail dynamic hazards, function hazards, and essential hazards in combinational networks. [16]

OR

Q.4 (a) What are stable and unstable states. Explain the concept of races and race-free assignments in detail. [10]

(b) Write short note on compatibility and state reduction procedure. [6]

UNIT – V

Q.5 Explain following incorporate with field programmable gate arrays. [8×2=16]

(a) Logic elements & programmability.

(b) Interconnect structures & programmability.

OR

Q.5 Write short notes on - [8×2=16]

(a) Extended Logic elements in FPGA.

(b) Flash Memory & anti-fuse configuration in FPGA.
