3E1653

Roll No. _____ Total No of Pages: 7

3E1653

B. Tech III Sem. (Main) Exam. Jan. 2016
Electronic Instrumentation & Control
3EI3 Digital Electronics
Common to EC & EIC

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination.

1. _____ 2. _____

UNIT-I

Q.1 (a) Convert the following - [4×1=4]

(i) $(2F\ 9A)_{16} = (\quad)_2$

(ii) $(1100100)_2 = (\quad)_8$

(iii) $(247.05)_{10} = (\quad)_2$

(iv) $(1010.011)_2 = (\quad)_{10}$

(b) Represent decimal no $(190)_{10}$ in following - [3×2=6]

(i) Excess – 3 code

(ii) Gray code

(iii) BCD code

(c) Perform the following operations - [3×2=6]

(i) $(11.1001)_2 - (01.110)_2$ using 2's complement

(ii) $(2AC)_{16} + (10F)_{16}$

(iii) $(32)_8 + (67)_8$

OR

Q.1 (a) Define the following with one example - [4×2=8]

(i) Error correcting codes

(ii) Gray code

(iii) Hamming distance

(iv) Even and odd parity code.

(b) Consider following codes - [4×2=8]

Code A	Code B	Code C	Code D
0001	000	01011	000000
0010	001	01100	001111
0100	011	10010	110011
1000	010	10101	
	110		
	111		
	101		
	100		

Deform which of the following properties is satisfied by each above codes.

(i) Detects single error

(ii) Detects double error

(iii) Corrects single error

(iv) Corrects single error and detects double error.

UNIT-II

Q.2 (a) Define the following of logic families -

(i) Fan – out

(ii) Figure of merit

(iii) Noise Immunity

(iv) Wired – logic.

(b) A DTL NAND gate is shown in fig – 2. Calculate its - [4×2=8]

(i) Fan out

(ii) Noise margin

(iii) Average power dissipated by the gate.

(iv) Logic levels v (0) & v (1)

Assume diode parameter $V_D \approx 0.7$ V (diode on voltage)

V_Y (cut in voltage) = 0.6V

Transistor parameter Cut in voltage $V_y = 0.5V$

$V_{BESat} \approx 0.8$volt.

$V_{CESat} \approx 0.2$volt.

hFE = 50 $V_{CC} = 9v$

$R = 10K\Omega$

$R_B = 50K\Omega$

$R_C = 3K\Omega$.

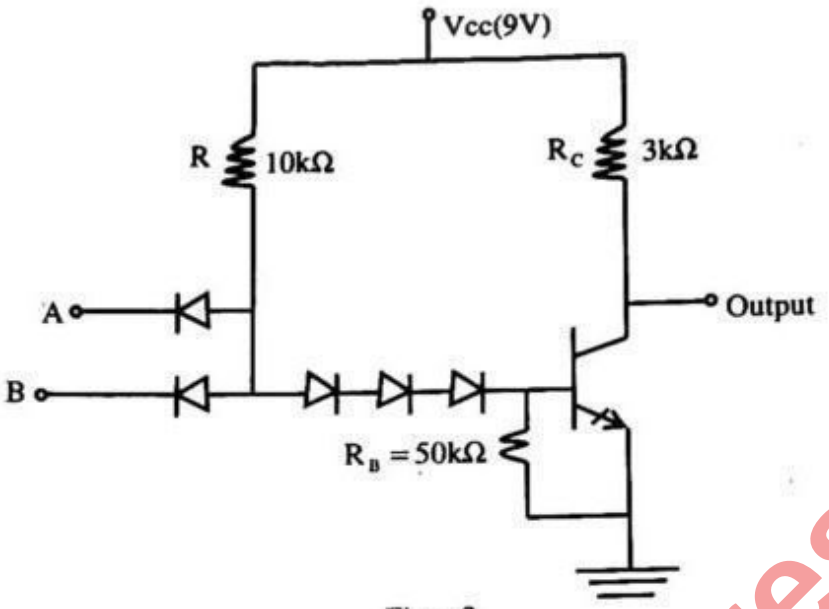

Fig = 2

OR

Q.2 (a) Explain the use of following in logic families - [4×2=8]

(i) Clamping diodes.

(ii) Open collector & open emitter outputs

(iii) Schottky diode

(iv) Totem pole output.

(b) Draw the circuit diagram of following - [4×2=8]

(i) 2 input HTL NAND gate

(ii) 2 input ECL OR gate

(iii) I^2L inverter

(iv) Q input NMOS OR gate (with Active load)

UNIT-III

Q.3 (a) minimize the logic expression with K – map [4×2=8]

(i) $F(A, B, CD) = \sum m(1, 2, 3, 7, 11, 15)\ fd(0, 4, 5)$

(ii) F (AB, CD) πm (1, 4, 6, 9, 10, 11) * d (13, 14, 15)

(b) What is Qvine – McCluskey minimization technique? Explain for minimize the function. [8]

$y(A, B, CD) = \sum m(0, 1, 3, 4, 5, 7, 8, 9, 11, 15)$

OR

Q.3 (a) minimize the following logic using K – map. [3×4=12]

(i) $y = AB(D + \overline{C}) + DC(\overline{A} + \overline{B}) + \overline{A}CD$

(ii) $y = \sum m(0, 1, 3, 5, 6)$

(iii) $\overline{y} = A \oplus B \oplus \overline{A}$

(b) What is multilevel K – map? Draw two – level K – map for five variable and show the group formation of 16 – adjacent ones in it. [4]

UNIT-IV

Q.4 Implement the following expression - [4×4=16]

(i) $y = A\overline{B}C$ using 2 input NAND only.

(ii) $y = \sum m(0, 2, 3, 6, 8, 9, 12, 14)$ using multiplexer

(iii) $y = \sum m(2, 3, 9, 11)$ using 4 to 16 line decoder.

(iv) 16×1 mux using 2×1 mux.

OR

Q.4 **Draw the logic diagram of and show all implementation steps.** [4×4=16]

(i) BCD to excess – 3encoder

(ii) 4 bit binary serial adders

(iii) 2 bit multiplier

(iv) Parity Generator 2 checkers (4bit)

UNIT-V

Q.5 (a) Draw the excitation table of - [2×2=4]

(i) JK FE

(ii) T – EF

(b) *Design a 4bit synchronous counter* [6]

(c) Obtain the output for the sequential circuit shown in Fig – 5 (a) [6]

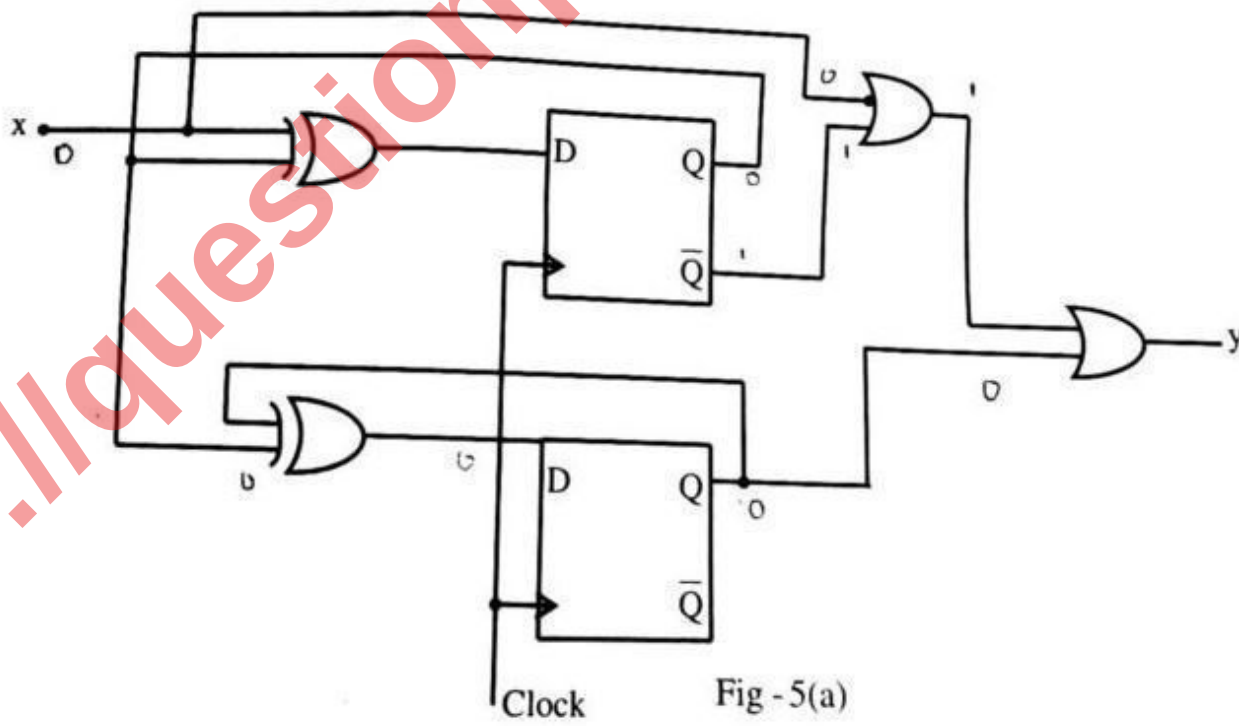

Fig - 5(a)

OR

Q.5 (a) Draw the state diagram of logic circuit shown fig – 5(a). [8]

(b) Design a logic circuit for the state diagram show in fig – 5(b). [8]

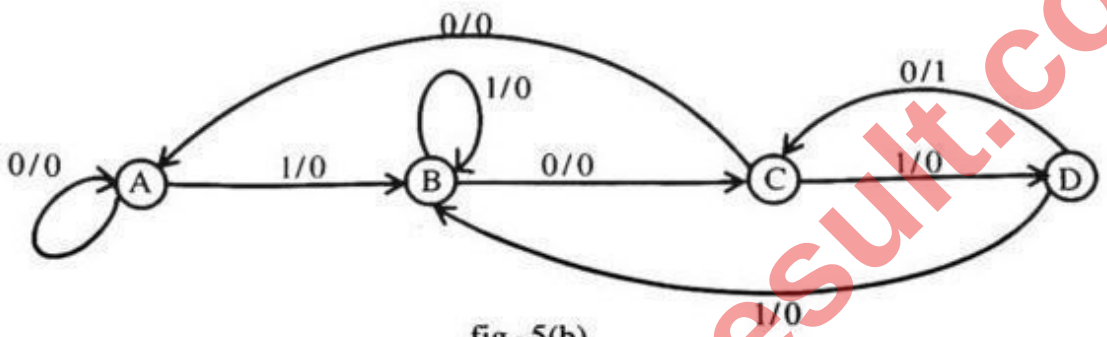

fig - 5(b)
