

5E5022

Roll No. _____

Total No of Pages: **4****5E5022**

B. Tech. V Sem. (Main / Back) Exam., Dec. 2014
Electronics and Communication Engineering
5EC2A Linear Integrated Circuits
(Common for EC, EI)

Time: 3 Hours**Maximum Marks: 80****Min. Passing Marks: 24***Instructions to Candidates:*

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination.

1. NIL2. NIL**UNIT – I**

Q. 1 (a) The following specifications are give for the dual input, balanced output bipolar differential amplifier:-

$R_C = 2.2k\Omega$, $R_E = 4.7k\Omega$, $R_S = 50\Omega$, $V_{CC} = 10V$, $V_{EE} = -10V$ and $\beta_F = \beta_o = 100$.

Assume $V_{BE} = 0.7V$. Find –

- (i) I_{CQ} and V_{CEQ}
- (ii) Differential- mode voltage gain ϕ
- (iii) Input and output resistances.

[10]

(b) For Fig- (1) –

$R_1 = R_2$, Slew rate = 50V/MS, $s_i = 10 \sin \omega t$

Find f_{max} for undistorted output.

[6]

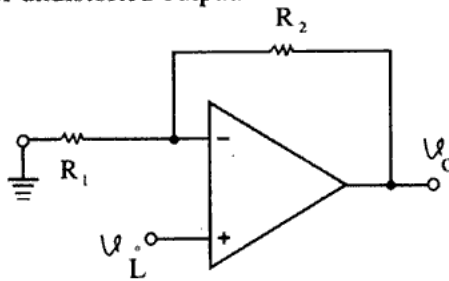


Fig-(1)

OR

(a) A Bipolar differential amplifier uses a BJT having $\beta_o = 200$ and biased at $I_{CQ} = 100 \text{ MA}$. Determine R_C and R_E so that $|A_{dm}| = 500$ and $\text{CMRR} = 80 \text{ dB}$. [10]

(b) Draw only output waveform with voltage level for fig- (2) –

$V_Z = 5.1\text{V}$, $V_D = 0.7\text{V}$, supply = $\pm 15\text{V}$

[6]

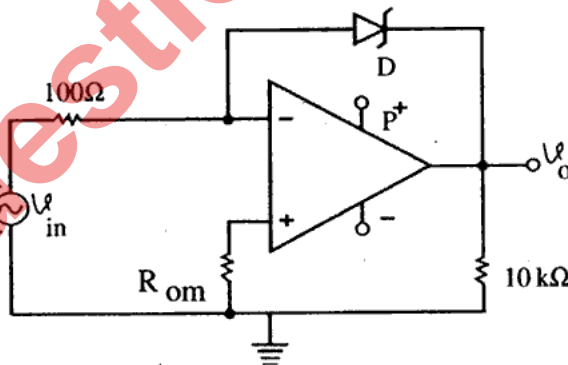


Fig-(2)

UNIT-II

- Q. 2 (a) Draw only circuit diagram of a square wave oscillator and design it for –
 $f_0 = 1\text{KHZ}$ using 741 ϕ , supply = $\pm 15\text{V}$. [8]
- (b) Draw the circuit diagram and explain the working of a voltage controlled-oscillator. [8]

OR

Design the following and also draw the – circuit diagrams of:-

- (a) Wein bridge oscillator- $f_0 = 2\text{KHZ}$, amplifier's gain = 5 [8]
- (b) Phase shift oscillator- $f_0 = 2\text{KHZ}$, amplifier's gain = 32 [8]

UNIT-III

- Q. 3 Explain first and second- order switched capacitor filters with required circuits. Also find relations between f_0 , f_{CLK} and capacitors. Mention the effect of stray capacitances and how stray capacitance errors can greatly reduce. [16]

OR

- (a) Draw and explain twin- T narrow band reject filter (Notch filter). [8]
- (b) Design a second-order low pass Butterworth filter (Takes care of guaranteed Butterworth response) for a cutoff frequency of 2KHz. Also draw the circuit diagram. [8]

UNIT-IV

- Q. 4 (a) Explain following with required diagram and waveforms using multiplier.
- (i) Frequency doubling. [4]
- (ii) Square root. [4]
- (b) Draw and explain 555 as table multi-vibrator. [8]

OR

Draw the output waveform and explain the working of fig-(3) and fig-(4).

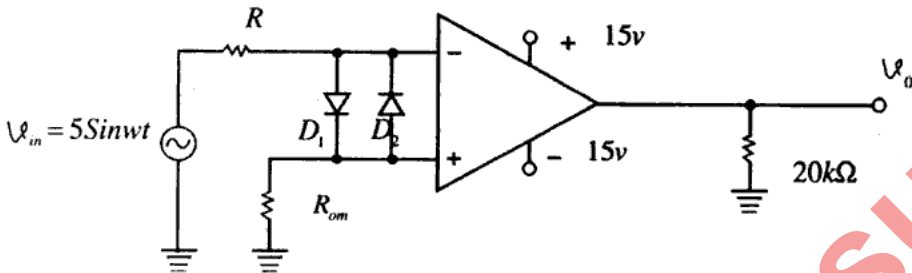


Fig.-3

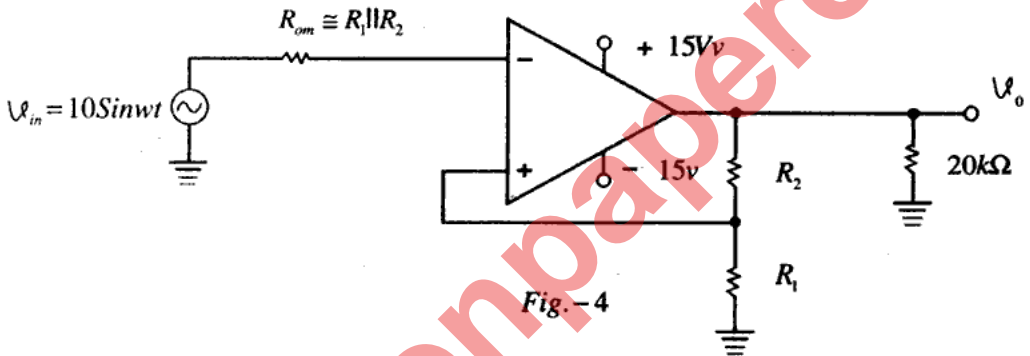


Fig.-4

UNIT-V

- Q. 5 (a) Draw and explain the working of an Antilog amplifier using diode. [8]
- (b) A PLL has a VCO with $K_0 = 20 \text{ KHz/V}$ and $f_c = 50 \text{ KHz}$. The amplifier gain is $A = 2$ and the phase detector has a maximum output voltage swing of $\pm 0.7\text{V}$. Find the lock range of the PLL. Assume gain equal to unity. [8]

OR

- (a) Draw the block diagram of PLL and explain working in detail. [10]
- (b) Explain FSK demodulator using PLL. [6]