7E7086

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B. Tech. VII Sem. (Main/Back) Exam., Nov – Dec. 2017
Electronics & Communication Engineering
7EC6.3A VHDL

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT-I

Q.1 (a) Differentiate between synthesis and simulation process in VHDL. [6]

(b) List the advantages of VHDL for digital design over the traditional methods. [6]

(c) Describe Design flow of ASICs. [4]

OR

Q.1 (a) Assume that a gate array exists in which the logic cell used is a three inputs NOR gate. The inputs to each NOR gate can be connected to either 1 or 0, or to any logic signal. Show how the following logic functions can be realized in the gate array. (Use Demorgan's theorem). [12]

(i) $f_1 = (x_1 + x_3)(x_2 + \bar{x}_3)$

(ii) $f_2 = (x_2 + \bar{x}_3)(x_1 + \bar{x}_2 + x_3)$

(b) Describe History of various Hardware Description Languages in brief manner. [4]

UNIT-II

Q.2 (a) Consider the following VHDL assignment statements [12]

$F_1 <= ((x_1 \text{ and } x_3) \text{ or } (\text{not } x_1 \text{ and not } x_3))$

and $((x_2 \text{ and } x_4) \text{ or } (\text{not } x_2 \text{ and not } x_4))$;

$F_2 <= (x_1 \text{ and } x_2 \text{ and not } x_3 \text{ and not } x_4) \text{ or}$

$(\text{not } x_1 \text{ and not } x_2 \text{ and } x_3 \text{ and } x_4) \text{ or}$

$(x_1 \text{ and not } x_2 \text{ and not } x_3 \text{ and } x_4) \text{ or } (\text{not } x_1 \text{ and } x_2 \text{ and } x_3 \text{ and not } x_4)$;

(i) Write complete VHDL code to implement f_1 & f_2.

(ii) Draw its timing simulation waveforms.

(b) What is the difference between signals and data types? Mention in tabulation form. [4]

OR

Q.2 (a) (i) What do you mean by architectures and RTL schematics? [3]

(ii) Explain different types of architectures with examples. [3]

(iii) What are sizes of entity and architecture which is defined in VHDL coding? [2]

(b) Write short notes on any two: [2×4=8]

(i) Packages

(ii) Simulation approaches

(iii) Elaboration signal drivers simulator kernel process

UNIT-III

Q.3 (a) Write VHDL code that represents a BCD to 7–segment decoder. Also draw its timing simulation waveforms. [8]

(b) Describe multiplexer synthesis using Shannon's expansions by explaining implementation of the three input majority function using a 4 to 1 multiplexer. [8]

OR

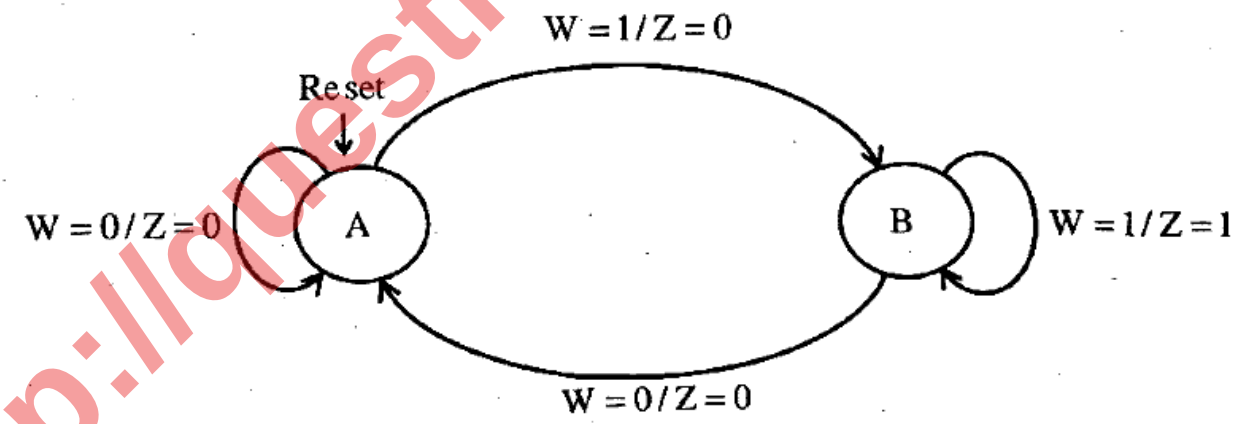
Q.3 (a) Write VHDL code for implementing D flip–flop using a WAIT–UNTIL statement. [8]

(b) What do you mean by counters? How many types of counters are there? Write their name. Write VHDL code for a down counter. [6]

(c) Define n – bit shift register. [2]

UNIT-IV

Q.4 (a) Write VHDL code for given state diagram of mealy type finite state machine. [8]



(b) Tabulate comparisons between synchronous and Asynchronous sequential circuits. [6]

(c) Define state diagram and state table. [2]

OR

Q.4 (a) What are the differences between Mealy and Moore Machines? Mention in tabular form. [4]

(b) What do you mean by vending machine controller? Explain its working and specifications. [4]

(c) Write VHDL code for Moore type FSM. [8]

UNIT-V

Q.5 (a) Write VHDL code for a n- bit register with an enable input. [12]

(b) Explain and draw data path circuit for the multiplier. [4]

OR

Q.5 (a) Explain clock synchronization using tristate buffers in the data path circuit. [8]

(b) Describe CPU organization and also explain its design concepts. [8]