

7E 4048

Roll No. _____

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7E 4048**B.Tech. VII Semester (Main/Back) Examination - 2014****Electronics & Comm. Engg.****7EC5 VLSI Design****Time : 3 Hours****Maximum Marks : 80****Min. Passing Marks : 24****Instructions to Candidates:**

Attempt any **five** questions, selecting **one** question from each **unit**. All questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.)

Unit - I

1. a) Draw the MOS transistor circuit model. Give the justification for all the capacitance. Compare the different capacitance (8)
- b) Provide comparative discussion of 'Twin - Tub CMOS fabrication' and 'Silicon - on - insulator' fabrication process. (8)

OR

1. a) Derive the V - I characteristics of enhancement MOSFET
 - i) Ohmic region
 - ii) Saturation region(8)
- b) Explain the NMOS fabrication process in detail. (8)

Unit - II

2. a) What are second order effect? Explain channel length modulation effects in detail. (8)
- b) Explain significance of (β_n / β_p) ratio of CMOS inverter. (8)

OR

2. a) Show that an inverter driven directly from the output of another inverter should have a Z p.u./ Z p.d. ratio of 4/1. (8)
- b) What are the factor which affects the threshold voltage? Derive expression for threshold voltage. (8)

Unit - III

3. a) Draw the corresponding circuit diagram for logic function. $Y = \overline{(A+B)} \cdot (C+D)$. Also calculate equivalent W/L ratio for NMOS and PMOS. Assume that $(W/L)_p = 20$ for all PMOS transistor and $(W/L)_n = 10$ for all NMOS transistor. (8)
- b) Explain CMOS transmission gate? Draw two input multiplexer circuit using it. (8)

OR

3. a) Explain and derive the expression for different type of power dissipation in CMOS circuit. (8)
- b) Implement the function F by using CMOS transmission gate $F = ABC + \overline{BC} + \overline{AB}$. (8)

Unit - IV

4. a) Draw the layout of given function and then optimize the same with the help of Euler's graph. $F = \overline{A \cdot (D+E)} + (B \cdot C)$ (8)
- b) Explain different types of layout design rules and compare them with applications? rtuonline.com (8)

OR

4. a) Draw stick diagram layout for : (8)
- i) 2 - input CMOS NAND Gate
- ii) EX - OR gate.
- b) Design layout for an n-diff wire connected to p - diff wire (8)

Unit - V

5. a) What type of language is VHDL? Explain advantages and limitations of VHDL language. (8)
- b) Write VHDL code for 4 : 1 multiplexer in behavioural style of modelling. (8)

OR

5. a) What is package? Differentiate between function and procedure. (8)
- b) Write VHDL code for
- i) J - K Flip - Flop
- ii) Full Adder using Half Adder. (8)