7E7084

Roll No. _____ Total No of Pages: 4

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B. Tech. VII Sem. (Main) Exam., Nov.-Dec.-2016
Electronics &Communication Engineering
7EC5A VLSI Design

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) The Process Parameters for an NMOS are

oxide thickness $t_{ox} = 500A^{\circ}$

substrate doping $M_A = 10^{16}/cm^{+3}$

Polysilicon gate doping $M_D = 10^{20}/cm^3$

Oxide interface fixed charge density $= 2 \times 10^{10}/cm^3$.

Calculate the Threshold Voltage V_T for it. [10]

(b) Discuss following High order effects in MOSFET -

(i) narrow channel effect [3]

(ii) sub threshold conduction [3]

OR

Q.1 (a) Draw all fabrication steps to achieve following inverter (fig. 1) [8]

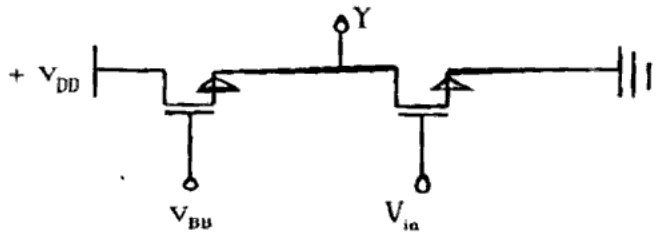

Fig – 1

Starts the fabrication using n – type substrate.

(b) Calculate the Junction capacitance at drain end in a NMOS shown in fig – 2 [8]

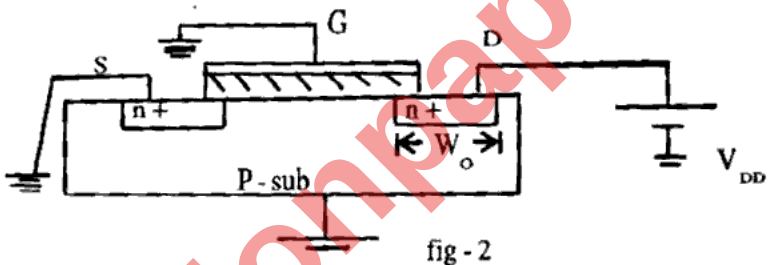

fig - 2

With substrate doping $N_A = 10^{12} / cm^3$

drain doping $N_D = 10^{18} / cm^3$

Junction depth $X_j = 0.1km.$

Drain Pellet is square of size $w_o \times w_o = (0.01 \times 0.01)\ km^2$

UNIT – II

Q.2 (a) Define noise margin for low and noise margin for high. Calculate these value for a CMOS inverter having $V_{tn} = |V_{tp}| = 0.8$, $\frac{K_n}{K_p} = 2.5$, and supply is $V_{DD} = 5$ volt. [8]

(b) Draw CMOS logic circuit for realize $y = \overline{[A(B+C)]\ (DEE)} = \overline{ADE\ (B+C)}$. Also set the (W/L) of each NMOS and PMOS such that the equivalent ratio of $\frac{K_n}{K_p} = 4$. [8]

OR

Q.2 (a) Draw the edge triggered D – Latch using CMOS logic. [6]

(b) Draw 4×1 Mux using transmission gate. Also compare the total no. of transistor required for such Mux using CMOS and TG. [6]

(c) Define power delay product (PDP) and energy delay product (EDP). Discuss why these parameters are called Figure of Merit for logic circuit. [4]

UNIT – III

Q.3 (a) Draw the Layout using possible Euler path for $y = \overline{(A+BC)\ (D+E)}$ [8]

(b) Draw the 2 × 1 Mux Layout using TG. [8]

OR

Q.3 (a) What are DRC rules for Layout? State any six DRC rules. Why we need to follow DRC rules when draw layout for any logic circuit? [6]

(b) Draw the Layout for a Half Adder using CMOS logic. [6]

(c) Draw Latch – up formation in CMOS inverter. [4]

UNIT – IV

Q.4 Draw following & explain their working- [4×4=16]

(a) SRAM cell

(b) DRAM cell

(c) $y = \overline{(AB+C)}$ using Domino logic

(d) Any NP (zipper) logic

OR

Q.4 (a) Explain the pre-charge and evaluation logic and explain zero transfer in detail. [8]

(b) What is C^2MOS logic? Draw any logic circuit using it. What are additional advantages of such logic? [8]

UNIT – V

Q.5 (a) Write the difference between custom design and FPGA in respect of design time and cost. [8]

(b) Write VHDL code for 2 input NAND and NOR gate. [8]

OR

Q.5 Write short note on any two - [2×8=16]

(i) ASIC Design

(ii) VHDL code for FF

(iii) Difference between First and Back End design.
