7E7084

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B. Tech. VII Sem. (Main/Back) Exam., Nov– Dec.2017
Electronics & Communication Engineering
7EC5A VLSI Design

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*
Units of quantities used/calculated must be stated clearly.
Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT-I

Q.1 (a) Explain the NMOS fabrication process with suitable diagrams. [8]

(b) An enhancement type NMOS transistor with $V_t = 0.7V$ conducts I_D 100 µA when $V_{GS} = V_{DS} = 1.2V$. Find the value of I_D for V_{GS} 1.5V and V_{DS} 3V. Also calculate the value of drain to source resistance r_{ds} for small $V_{DS} = V_{GS} = 3.2V$. [8]

OR

Q.1 (a) Find the relationship between drain to current source (I_{ds}) to voltage (V_{ds}) in non -saturated region. [8]

(b) What are various second order effect? Discuss how many have been included into device model of MOS transistor? [8]

UNIT-II

Q.2 (a) Determination of pull up to pull down ratio $[Z_{Pu}/Z_{pd}]$ for NMOS inverter driven by another NMOS inverter. [8]

(b) Design the following logics using CMOS:

(i) $Y = ABC + \overline{ABC}$ [4]

(ii) $Y = AB\overline{C} + \overline{A}BC$ [4]

OR

Q.2 (a) Describe the structure of CMOS transmission gate. Explain why such a gate is desirable to control transmission of signal rather than single transistor? [8]

(b) What is noise margin? Explain the procedure to determine noise margin? [8]

UNIT-III

Q.3 (a) Draw the stick diagram layout for –

(i) 2 input CMOS NAND gate [4]

(ii) 2 input CMOS NOR gate [4]

(b) Explain the layout design rules. [8]

OR

Q.3 (a) Explain the layout for NAND gate with suitable example. [8]

(b) Find the network graph and common Euler path for PMOS and NMOS network in the given function $F = \overline{A + BC}$ [8]

UNIT-IV

Q.4 (a) Compare the SRAM and DRAM cell. [8]

(b) Explain various types of memories. [8]

OR

Q.4 (a) Define clocked CMOS logic and its advantages. [8]

(b) Briefly explain NORA and NP (zipper) logic. [8]

UNIT-V

Q.5 (a) Write a VHDL code for-

(i) J. K flip flop [4]

(ii) T flip flop [4]

(b) Explain the ECAD tools for first back design. [8]

OR

Q.5 (a) Write short note on:

(i) Behavioral Modelling [4]

(ii) Structural Modelling [4]

(b) Write a VHDL code for structural modelling of full Adder. [8]
