8E8021

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B.Tech. VIII Semester (Main/Back) Examination, April/May -2017
Electronics and Communication Engg.
8EC1A IC Technology

Time : 3 Hours

Maximum Marks : 80
Min. Passing Marks : 26

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitable by assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

Unit-I

1. a) List out the steps of EGS preparation with suitable diagrams. How will you recover HCL and trichlorosilane. **(12)**

   b) Discuss about getting treatments. **(4)**

OR

1. a) Explain silicon shaping and wafer preparation. **(8)**

   b) Draw the czochralski growth reactor. **(4)**

   c) Discuss 4 point probe technique for resistivity measurement. **(4)**

Unit-II

2. a) State and explain pick's first law and second law. **(8)**

   b) Draw and explain linear and parabolic rate co-efficient. **(8)**

OR

2. a) Define the term diffusion.Explain Ion implantation system with suitable diagrams. **(12)**

   b) What are oxide properties? **(4)**

Unit-III

3. a) Explain the physical significance of chemical equilibrium and the law of mass action. Discuss the phenomena by taking an example. **(12)**

   b) What are the possible defects that could occur in an epitaxial growth. **(4)**

OR

3. a) Explain the process of Molecular Beam epitaxy in detail. Discuss the utility of khudcell with diagram. **(10)**

   b) Draw the hot wall reactor and cold wall reactor of LPCVD. **(6)**

Unit-IV

4. a) Define the term lithography and optical lithography. Explain the process of projection printing. **(8)**

   b) What are the types of photoresist and their chemical composition? Describe the growth system for DQ photo resist and ketone formation. **(8)**

OR

4. a) Explain the process of reaction Ion etching with suitable diagram. **(10)**

   b) Draw the flow chart of Mask generation. **(6)**

Unit-V

5. a) What are the fundamental consideration for IC processing? **(8)**

   b) Draw the processing steps of NMOS IC technology. **(8)**

OR

5. Write short note on : **(2×8)**

   a) LOCOS method

   b) Metallization and planarization