

3E1481

Roll No. : _____

Total Printed Pages : **4****3E1481**

B. Tech. (Sem. III) (Main & Back) Examination, January - 2013
Electrical Engg.
3EE1 Power Electronics - I

Time : 3 Hours]

[Total Marks : 80
[Min. Passing Marks : 24

*Attempt any five questions, selecting one question from each unit.
All questions carry equal marks. Schematic diagrams must be
shown wherever necessary. Any data you feel missing suitably be
assumed and stated clearly.*

Units of quantities used/ calculated must be stated clearly.

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. Nil _____ 2. NIL _____

UNIT - I

- 1 (a) Consider on open circuited P-n junction. Sketch curves as a function of distance across the junction of space charge, electric field and potential. 8
- (b) Explain zener break down. Also explain working of a zener diode. 8

OR

- 1 (a) How does the dynamic resistance 'r' of a diode vary with
(i) Current and
(ii) Temperature
(iii) What is the order of magnitude of r for silicon at room temperature and for a dc current of 1mA ? 8
- (b) Explain photo diodes. Does there is any relationship between Photo Diodes and Solar Cell ? 8

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[Contd...

UNIT - II

- 2 (a) What are electronics filters ? Explain various types of filters with their applications.

8

- (b) Explain single phase full wave bridge rectifiers. Can the transformer and the load be interchanged in it ?

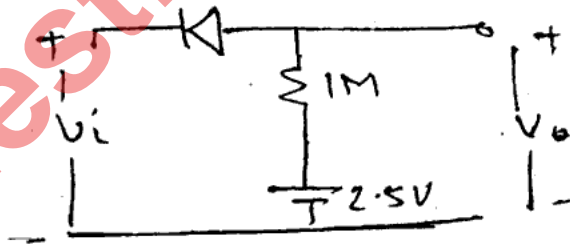
8

OR

- 2 (a) Prove that the regulation of both the half wave and full wave rectifier is given by $\frac{R_f}{R_L} \times 100\%$

$$\% \text{ Regulation} = \frac{R_f}{R_L} \times 100\%$$

- (b) A symmetrical 5K Hz square wave whose output varies between + 10 and - 10V is impressed upon the clipping circuit shown. Assume $R_f = 0, R_r = 2M$.



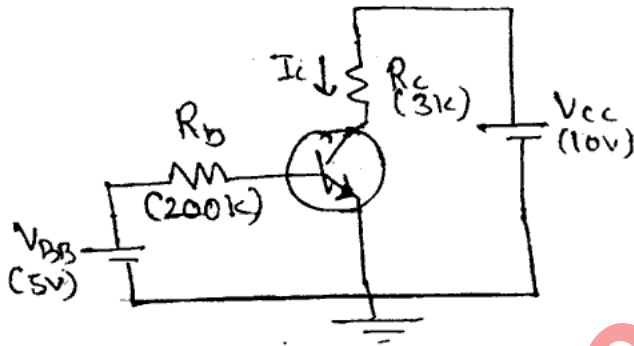
UNIT - III

- 3 (a) Sketch the hybrid h-model for CE configuration and find the expression for r_{bce} , S_m and r_{ce} in terms of h-parameter constant of a transistor.

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- (b) Find the transistor current in the circuit of fig below a silicon transistor with $\beta = 100$ and $I_{CO} = 20 \text{ nA} = 2 \times 10^{-5} \text{ mA}$ is under consideration.

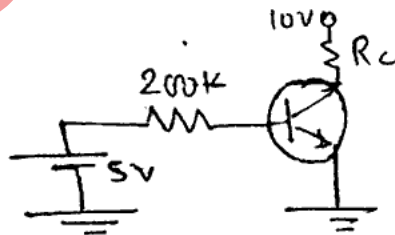


OR

- 3 (a) Explain concept of minority carrier concentration in the base for cutoff, active and saturation conditions in a BJT.

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- (b) A silicon transistor with $V_{BE,sat} = 0.8 \text{ V}$, $\beta = h_{FE} = 100$, $V_{CE,sat} = 0.2 \text{ V}$ is used in the circuit shown. Find the minimum value of R_C for which the transistor remain in saturation.



UNIT - IV

- 4 (a) Explain construction, working and V-I characteristics of a JFET.

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- (b) Explain DC analysis of FET, also explain FET as a voltage variable resistor.

8

OR

- 4 (a) Explain MOSFET with its type, construction and V-I characteristics ?

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- (b) The amplifier shown in fig utilized an n-channel FET for which $V_p = -2.0\text{ V}$ and $I_{DSS} = 1.65\text{ mA}$. It is desired to bias the circuit at $I_D = 0.8\text{ mA}$, using $V_{DD} = 24\text{ V}$. Assume $r_d \gg R_d$ find

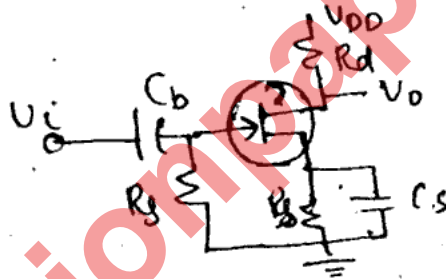
(a) V_{GS}

(b) g_m

(c) R_s

(d) R_d

such that the voltage gain is at least 20 dB, with R_s bypassed with a very large capacitance C_s .



UNIT - V

- 5 (a) Sketch the circuit for Darlington pair and find its overall current gain with help of its ac equivalent circuit.

8

- (b) Explain frequency response of CE transistor as amplifier at high frequency.

8

OR

- 5 Write short notes on any two :

16

(a) Bootstrapped Darlington circuit

(b) Miller's theorem and its dual

(c) Cascaded BJT amplifiers.

