8E8046

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B.Tech. VIII Semester (Main/Back) Examination, April/May-2017

Electrical and Electronics Engineering

8EX4.3A VHDL

Time : 3 Hours **Maximum Marks : 80**

Min. Passing Marks : 26

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitable by assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

Unit-I

1. a) What is the history of VHDL? **(8)**

   b) What are the five design constructs of VHDL? Explain briefly. **(8)**

OR

1. a) Explain briefly various types of data-types in VHDL? **(8)**

   b) Explain briefly various types of operators in VHDL. **(8)**

Unit-II

2. a) Write a program of 4:1 multiplexer in VHDL? **(8)**

   b) Write VHDL program of binary to grey convertor with diagram. **(8)**

OR

2. a) Draw and explain BCD to 7-segment display decoder with diagram. **(8)**

   b) Write VHDL program of 2 to 4 decoder with diagram. **(8)**

Unit-III

3. a) Write VHDL program of JK flip flop with diagram. **(8)**

   b) Write VHDL program of D flip flop with diagram. **(8)**

OR

3. a) Write VHDL program of 4-bit shift register with diagram. (8)

b) Draw and explain sequential circuit with diagram. (8)

Unit-IV

4. a) What Finite State Machine (FSM)? Explain mealy and moore type FSM. (4+4=8)

b) Design a synchronous sequential circuit using D flip flop for sequence detector, that detect the occurence of particular pattern on its input and that follows below condition : (8)

- One input w, one output z, circuit and positive edge triggered,

- The output z =1, if during two immediate preceding clock cycles the input 'w' was equal to 1, otherwise z = 0?

OR

4. a) Write VHDL code of serial adder. (8)

b) Explain vending machine using state diagram and block diagram. (8)

Unit-V

5. a) Draw and explain CPU organization and its design concepts. (8)

b) Draw and explain clock synchronization. (8)

OR

5. a) Draw the schematic diagram for the data path circuit for the sort operation. (8)

b) What is memory organization? Draw a diagram of a single SRAM cell. (4+4=8)